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PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. 219.003-US)

In the Application of: **Yamada**

Serial No: **09/865,528**

Filed: **May 29, 2001**

Title: **Semiconductor Device Test Method and Semiconductor Device Tester**

) Group Art Unit: **2829**
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) Before Examiner: **V. Nguyen**
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)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 28, 2004
Date
Michiko Sites
(person signing this certificate)
Michiko Sites
Signature

SUBMISSION OF ENGLISH TRANSLATIONS

Dear Sir:

Attached hereto is an English translation of each of the following Japanese patent applications: JP50-63990, JP57-6310, JP62-19707, which were submitted in an Information Disclosure Statement dated March 17, 2004.

Respectfully submitted,

Date: May 28, 2004

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650-968-8079